DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 8/29/2011, with respect to claims 1, 4-6, 9, and 11-12, have been considered but are moot in view of the new ground(s) of rejection.

2. The amended independent claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise et al (U.S. Pub. 2003/0156652 A1), and in view of Parameswaran et al (U.S. Pub. 2005/0262510 A1). Parameswaran et al teaches amended additional feature (paragraphs [0071], multiple processing units run in parallel in a pipeline; paragraph [0075], Multi-threaded pipeline spanning multiple macroblocks), see claim rejections below. The combination of Wise et al and Parameswaran et al renders claims 1 and 9 obvious to one of ordinary skill in the art at the time of the invention. The same rationale applies to the dependent claims. Therefore claims 1, 4-5, 9, and 11-12 remain rejected. The amended independent claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales et al (U.S. 5,289,577 A), and in view of Wise et al and Parameswaran et al. The combination of Gonzales et al, Wise et al, and Parameswaran et al renders claim 6 obvious to one of ordinary skill in the art at the time of the invention. Therefore claim 6 remains rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise et al (U.S. Pub. 2003/0156652 A1), and in view of Parameswaran et al (U.S. Pub. 2005/0262510 A1).

5. Regarding claim 1, Wise et al teaches an image data-processing apparatus (paragraph [0002], "improvements in methods and apparatus for decompression which operates to decompress and/or decode a plurality of differently encoded input signals"; "this embodiment relates to the decoding of any one or the well known standards known as JPEG, MPEG and H.251.". An apparatus to decode image data, e.g., JPEG, MPEG, is an image data-processing apparatus.) comprising:

an image data -decoding unit operable to allow input encoded data fed into said image data-processing apparatus to be decoded through pipeline processing, thereby providing decoded image data (paragraph [0002], decoding a plurality of differently encoded input signals; paragraph [0003], pipeline processor; paragraph [0046], outputting or displaying decoded image data.);

a pipeline controller operable to control the pipeline processing in said image data -decoding unit (paragraph [0003], pipeline processor; paragraph [0036], controlling processing stages) ; and

a memory operable to store the input encoded data and the decoded image data (paragraph [0037], primary and secondary storages; paragraph [0046], memory, storing and retrieving picture data.),

wherein a series of decoding processes are divided into a plurality of process stages (paragraph [0036], a plurality of processing stages),

wherein said image data-decoding unit includes a plurality of data processing units (see below: variable length decoding processing, inverse quantization processing, motion compensation processing), and

wherein said plurality of data processing units includes at least two (see below: variable length decoding processing, inverse quantization processing, motion compensation processing) of:

a variable length decoding processing unit operable to practice variable length decoding of the input encoded data, thereby providing quantized DCT coefficients and a motion vector (paragraph [0053], a spatial decoder for video data and having a Huffman decoder; paragraph [0139], variable length coding; paragraph [0116], 64 DCT coefficients (source, quantized or dequantized); also see paragraphs [0588] and [0590] for quantized DCT coefficients; see paragraphs [0129]-[0130] for motion vector.);

an inverse quantization processing unit operable to inversely quantize the quantized DCT coefficients from said variable length decoding processing unit, thereby providing inversely quantized DCT coefficients (paragraphs [0588] and [0590], inverse quantizer, and inverse DCT);

an inverse DCT processing unit operable to practice inverse DCT processing of the inversely quantized DCT coefficients from said inverse quantization processing unit, thereby providing DCT coefficients (This is similar to an inverse quantization processing unit above. In addition, the claim only requires two elements out of four. See other elements.) ; and

a motion compensation processing unit operable to generate decoded image data of a present frame using (i) the DCT coefficients from said inverse DCT processing unit, (ii) the motion vector from said variable length decoding processing unit, and (iii) decoded image data of a previous frame stored in said memory (paragraphs [0129]-[0130], motion compensation; paragraphs [0313]-[0314], "The output from the IDCT 83 is passed over line 84 to a temporal decoder"; "As a first output from the fork 91, the control tokens, e.g., motion vectors and the like, are passed over line 93 to an address generator 94.";.....; "The output from the output selector 106 is passed over line 109 to a Video Formatter."), and

wherein said pipeline controller includes:

a start-up table storage unit operable to contain a pipeline start-up table in which start-up information on control over the pipeline processing in said image data - decoding unit is registered (paragraph [1274], the quantization table memory is considered as a start-up table storage unit; paragraph [1278], the default quantization table for MPEG is considered as a pipeline start-up table.) ;

an offset-determining unit operable to determine an offset value for use in referencing the pipeline start-up table in said start-up table storage unit (paragraph [1280], offset from start of quantization table memory.);

a start-up stage-determining unit operable to read the start-up information from the pipeline start-up table in said start-up table storage unit in accordance with the offset value determined by said offset-determining unit, thereby determining a start-up method

for the pipeline processing in said image data -decoding unit (paragraphs [1278] and [1284], determining the start-up method, e.g., MPEG operations.) ; and

a pipeline control unit operable to control said offset-determining unit and said start-up stage-determining unit, thereby controlling the pipeline processing in said image data -decoding unit in accordance with the start-up method for the pipeline processing as determined by said start-up stage-determining unit (paragraphs [1288]-[1294], controlling the inverse discrete transform based on the quantization table values.).

6. However, Wise et al does not explicitly teach wherein said image data-decoding unit includes a plurality of data processing units, each of the plurality of data processing units performing, independently from the other plurality of data processing units, a process on a corresponding stage, from among the plurality of process stages, for a unit of a macro block, thereby practicing pipeline processing.

7. Parameswaran et al, in the same field of endeavor, teaches wherein said image data-decoding unit includes a plurality of data processing units, each of the plurality of data processing units performing, independently from the other plurality of data processing units, a process on a corresponding stage, from among the plurality of process stages, for a unit of a macro block, thereby practicing pipeline processing (paragraphs [0071], multiple processing units run in parallel in a pipeline; paragraph [0075], Multi-threaded pipeline spanning multiple macroblocks). Multiple processing units executing in parallel or independently increases the performance of the system.

8. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine apparatuses as shown Wise et al and Parameswaran et al for the benefit of increasing the performance of the system.

9. Regarding claim 9, Wise et al teaches an image data-processing method (paragraph [0002], "improvements in methods and apparatus for decompression which operates to decompress and/or decode a plurality of differently encoded input signals"; "this embodiment relates to the decoding of any one or the well known standards known as JPEG, MPEG and H.251.".) comprising:

Dividing a series of processes for processing image data into a plurality of process stages, thereby processing the image data through a pipeline (paragraph [0003], pipeline processor; paragraph [0036], controlling processing stages);

storing the processed image data (paragraph [0037], primary and secondary storages; paragraph [0046], memory, storing and retrieving picture data); and

controlling the pipeline (paragraph [0036], controlling processing stages),

wherein said processing image data includes a plurality of data processes (paragraph [0053], a spatial decoder for video data and having a Huffman decoder; paragraph [0139], variable length coding; paragraphs [0588] and [0590], inverse quantizer, and inverse DCT), and

wherein said controlling the pipeline includes:

storing a pipeline start-up table in which start-up information on control over start-up of the several staged pipeline is registered (paragraph [1274], the quantization table

memory is considered as a start-up table storage unit; paragraph [1278], the default quantization table for MPEG is considered as a pipeline start-up table.);

determining an offset value for use in referencing the pipeline start-up table (paragraph [1280], offset from start of quantization table memory.);

obtaining the start-up information from the pipeline start-up table based on the determined offset value, thereby determining a start-up method for the several staged pipeline (paragraphs [1278] and [1284], determining the start-up method, e.g., MPEG operations.); and

controlling the pipeline in accordance with the determined start-up method for the several staged pipeline (paragraphs [1288]-[1294], controlling the inverse discrete transform based on the quantization table values.).

10. However, Wise et al does not explicitly teach wherein said processing the image data includes a plurality of data processes, each of the plurality of data processes performing, independently of the other plurality of data processes, a process on a corresponding stage, from among the plurality of process stages, for a unit of a macro block, thereby practicing the pipeline.

11. Parameswaran et al, in the same field of endeavor, teaches wherein said processing the image data includes a plurality of data processes, each of the plurality of data processes performing, independently of the other plurality of data processes, a process on a corresponding stage, from among the plurality of process stages, for a unit of a macro block, thereby practicing the pipeline (paragraphs [0071], multiple processing units run in parallel in a pipeline; paragraph [0075], Multi-threaded pipeline

spanning multiple macroblocks). Multiple processes executing in parallel or independently increases the performance of the system.

12. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine methods as shown Wise et al and Parameswaran et al for the benefit of increasing the performance of the system.

13. Regarding claim 11, Wise et al teaches wherein said processing the image data through the pipeline includes :

decoding encoded data for each macro block (paragraph [0046], decoding data blocks; paragraph [0053], a spatial decoder for video data and having a Huffman decoder);

detecting a code error from the encoded data (paragraphs [0988]-[0989], error detection); and

practicing error concealment processing (paragraph [0996], concealing data communication error), and

wherein when a code error is detected at a macro block during said detecting the code error, said controlling the pipeline includes interrupting decoding processing for macro blocks subsequent to the macro block at which the code error has been detected, thereby practicing the error concealment processing (paragraphs [0994]-[0996], when Start Code Detector detects certain errors, it generates an interrupt. Then the error concealment processing is practiced.) .

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales et al (U.S. 5,289,577 A), and in view of Wise et al and Parameswaran et al.

15. Regarding claim 6, Gonzales et al teaches an image data-processing apparatus (Fig. 2, image data coding/decoding system) comprising:

an image data -encoding unit operable to allow input image data fed into said image data-processing apparatus to be encoded through pipeline processing, thereby providing encoded data (Fig. 2, and column 7, lines 9-12, encoding, image memory 22 to CODEC 24);

a pipeline controller operable to control the pipeline processing in said image data -encoding unit (column 4, lines 54-68, processing pipeline and pipeline control); and

a memory operable to store reconfigured image data corresponding to the input image data, and the encoded data (Fig. 2, and column 7, lines 9-12, image memory 22, and local memory 32),

wherein a series of encoding processes are divided into a plurality of process stages (Fig. 2, and column 7, lines 9-12, encoding; Fig. 1, Stage i-1 to Stage i+2),

wherein said image data-encoding unit includes a plurality of data processing units, wherein said plurality of data processing units include at least two (see below: motion compensation; DCT processing; quantization processing; variable length encoding) of:

a motion detection processing unit operable to detect a motion vector of a present frame, using (i) the input image data, which is input image data of the present frame, and (ii) reconfigured image data of a previous frame stored in said memory (see other four elements. The claim only requires two.);

a motion compensation processing unit operable to generate predicted image data of the present frame using (i) the motion vector detected by said motion detection processing unit and (ii) the reconfigured image data of the previous frame in said memory (column 13, lines 34-37, motion compensation. Motion compensation inherently requires motion vector detection.);

a DCT processing unit operable to practice DCT processing of a difference between the predicted image data generated by said motion compensation processing unit, and the input image data, thereby providing DCT coefficients (column 7, lines 27-42, DCT-based compression algorithm, and producing DCT coefficients.);

a quantization processing unit operable to quantize the DCT coefficients from said DCT processing unit, thereby providing quantized DCT coefficients (column 7, lines 38-42, quantizing DCT coefficients.);

an inverse quantization processing unit operable to inversely quantize the quantized DCT coefficients from said quantization processing unit, thereby providing inversely quantized DCT coefficients (see other four elements. The claim only requires two.);

an inverse DCT processing unit operable to practice inverse DCT processing of the inversely quantized DCT coefficients from said inverse quantization processing unit, thereby providing DCT coefficients for use in obtaining reconfigured image data (see other four elements. The claim only requires two.); and

a variable length encoding processing unit operable to practice variable length encoding of (i) the quantized DCT coefficients from said quantization processing unit

and (ii) the motion vector detected by said motion detection processing unit, thereby providing encoded data (column 7, lines 46-55, variable length encoding.).

16. However, Gonzales et al does not explicitly teach wherein said image data-decoding unit includes a plurality of data processing units, each of the plurality of data processing units performing, independently from the other plurality of data processing units, a process on a corresponding stage, from among the plurality of process stages, for a unit of a macro block, thereby practicing pipeline processing, and wherein said pipeline controller includes: a start-up table storage unit operable to contain a pipeline start-up table in which start-up information on control over the pipeline processing in said image data -encoding unit is registered; an offset-determining unit operable to determine an offset value for use in referencing the pipeline start-up table in said start-up table storage unit; a start-up stage-determining unit operable to read the start-up information from the pipeline start-up table in said start-up table storage unit in accordance with the offset value determined by said offset-determining unit, thereby determining a start-up method for the pipeline processing in said image data -encoding unit; and a pipeline control unit operable to control said offset-determining unit and said start-up stage-determining unit, thereby controlling the pipeline processing in said image data -encoding unit in accordance with the start-up method for the pipeline processing as determined by said start-up stage-determining unit.

17. Parameswaran et al, in the same field of endeavor, teaches wherein said image data-decoding unit includes a plurality of data processing units, each of the plurality of data processing units performing, independently from the other plurality of data

processing units, a process on a corresponding stage, from among the plurality of process stages, for a unit of a macro block, thereby practicing pipeline processing (paragraphs [0071], multiple processing units run in parallel in a pipeline; paragraph [0075], Multi-threaded pipeline spanning multiple macroblocks). Multiple processing units executing in parallel or independently increases the performance of the system.

18. Wise et al, also in the same field of endeavor, teaches wherein said pipeline controller includes:

a start-up table storage unit operable to contain a pipeline start-up table in which start-up information on control over the pipeline processing in said image data -decoding unit is registered (paragraph [1274], the quantization table memory is considered as a start-up table storage unit; paragraph [1278], the default quantization table for MPEG is considered as a pipeline start-up table.) ;

an offset-determining unit operable to determine an offset value for use in referencing the pipeline start-up table in said start-up table storage unit (paragraph [1280], offset from start of quantization table memory.);

a start-up stage-determining unit operable to read the start-up information from the pipeline start-up table in said start-up table storage unit in accordance with the offset value determined by said offset-determining unit, thereby determining a start-up method for the pipeline processing in said image data -decoding unit (paragraphs [1278] and [1284], determining the start-up method, e.g., MPEG operations.) ; and

a pipeline control unit operable to control said offset-determining unit and said start-up stage-determining unit, thereby controlling the pipeline processing in said image data

-decoding unit in accordance with the start-up method for the pipeline processing as determined by said start-up stage-determining unit (paragraphs [1288]-[1294], controlling the inverse discrete transform based on the quantization table values.). Wise et al discloses a system of video compression/decompression supporting multiple compression standards. The system provides enhanced flexibility, efficiency and performance.

19. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the apparatuses as shown in Gonzales et al, Parameswaran et al, and Wise et al because Multiple processing units executing in parallel or independently in Parameswaran et al increases the performance of the system, and Wise et al's system of video compression/decompression supports multiple compression standards and provides enhanced flexibility, efficiency and performance.

20. Claims 4-5, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise et al, and in view of Parameswaran et al, as applied to claims 1 and 11 above, and further in view of Lee (U.S. Pub. 2003/0117585 A1, already of record).

21. Regarding claim 4, the combination of Wise et al and Parameswaran et al remains as applied to claim 1 above. Wise et al also teaches further comprising an error concealment processing unit (paragraph [0996], concealing data communication error),

wherein said variable length decoding processing unit further includes a code error-detecting unit operable to detect a code error from the input encoded data (paragraphs [0988]-[0989], error detection).

22. However, the combination does not explicitly teach wherein, when said code error-detecting unit detects the code error at a macro block of the input encoded data, said error concealment processing unit applies previously decoded image data from said memory onto (i) the macro block at which the error has been detected and (ii) subsequent macro blocks, thereby concealing a disturbance caused by the code error in the input encoded data in decoded image display.

23. Lee, also in the same field of endeavor, teaches wherein, when said code error-detecting unit detects the code error at a macro block of the input encoded data, said error concealment processing unit applies previously decoded image data from said memory onto (i) the macro block at which the error has been detected and (ii) subsequent macro blocks, thereby concealing a disturbance caused by the code error in the input encoded data in decoded image display (paragraph [0243], "in case that a texture error occurred, the current frame is INTRA, no decoded DC coefficient exists, and it is impossible to use the DC coefficient of the adjacent upper block, the macroblock is replaced by the macroblock of the previous frame at the same location."). There are many types of error conditions. Lee listed thirteen error conditions and the corresponding concealing methods. Some method is most appropriate for certain error condition. The above method appears most appropriate for the detected error condition.

24. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the apparatuses as shown in Wise et al, Parameswaran et al, and Lee by applying previously decoded image data from said memory onto the macro block at which the error has been detected and subsequent macro blocks when

said code error-detecting unit detects the code error at a macro block of the input encoded data because this error concealing method is most appropriate for the detected error condition.

25. Regarding claim 5, Lee teaches wherein when said code error-detecting unit detects the code error at the macro block of the input encoded data, said error concealment processing unit excludes previously processed macro blocks from targets at which the disturbance in decoded image display is to be concealed, the previously processed macro blocks being processed earlier, by the plurality of process stages, than the macro block at which the error has been detected (Note: the examiner interprets the claim as the concealment process is only applied to the error data, it is not applied to the previously processed "good" data. In paragraphs [0210]-[0214], Lee teaches localizing the extent of an error-occurred location, and minimizing the length of the codes impacted by the error. That is, the error concealing process is only applied to the absolutely necessary blocks of the data.).

26. Regarding claim 12, the combination of Wise et al and Parameswaran et al remains as applied to claim 11 above. However, the combination does not explicitly teach wherein said practicing the error concealment processing includes applying previously processed image data that is stored by said storing the processed image data, thereby practicing the error concealment processing.

27. Lee, also in the same field of endeavor, teaches wherein said practicing the error concealment processing includes applying previously processed image data that is stored by said storing the processed image data, thereby practicing the error

concealment processing (paragraph [0243], "in case that a texture error occurred, the current frame is INTRA, no decoded DC coefficient exists, and it is impossible to use the DC coefficient of the adjacent upper block, the macroblock is replaced by the macroblock of the previous frame at the same location."). There are many types of error conditions. Lee listed thirteen error conditions and the corresponding concealing methods. Some method is most appropriate for certain error condition. The above method appears most appropriate for the detected error condition.

28. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the methods as shown in Wise et al, Parameswaran et al, and Lee by applying previously processed image data that is stored by said storing the processed image data, thereby practicing the error concealment processing because this error concealing method is most appropriate for the detected error condition.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIZE MA whose telephone number is (571)270-3709. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao M. Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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